WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cells each capable of storing and programming N-level data, where N is a natural number equal to or greater than 2;

a reference cell storing a reference level used when reading a data level stored in said memory cells;

a counter circuit counting number of times of reading of said reference cell; and

check means for determining whether said reference level stored in said reference cell is within a preset range when said number of times of reading that is counted by said counter circuit reaches a specified value.

2. The semiconductor memory device according to claim 1, wherein said counter circuit counts the number of times of reading of said reference cell in at least one of a read operation, a program operation, and an erase operation for said memory cells.

3. The semiconductor memory device according to claim 1, comprising correction means for, if said check means determines that said reference level is out of said range, correcting the reference level to fall within said range.

4. The semiconductor memory device according to claim 3, wherein said correction means corrects said reference level using a master reference level fixed to a master reference cell other than said reference cell.

5. The semiconductor memory device according to claim 4, wherein said master reference cell comprises a fixed resistance.

6. The semiconductor memory device according to claim 1, wherein

each of said memory cells and said reference cell comprises:

a nonvolatile variable resistance element whose electric resistance is changed by an electric stress and remains on the changed electric resistance even after said electric stress is removed; and

a select transistor.

7. The semiconductor memory device according to claim 6, wherein said nonvolatile variable resistance element has a manganese-containing oxide of a perovskite structure formed between electrodes.

8. A semiconductor memory device comprising:

a plurality of memory cells each capable of storing and programming N-level data, where N is a natural number equal to or greater than 2;

a reference cell storing a reference level used when reading a data level stored in said memory cells;

a timing generation circuit; and

check means for determining whether said reference level stored in said reference cell is within a preset range, in synchronicity with a synchronous signal output from said timing generation circuit.

9. The semiconductor memory device according to claim 8, comprising correction means for, if said check means determines that said reference level is out of said range, correcting the reference level to fall within said range.

10. The semiconductor memory device according to claim 9, wherein said correction means corrects said reference level using a master reference level fixed to a master reference cell other than said reference cell.

11. The semiconductor memory device according to claim 10, wherein

said master reference cell comprises a fixed resistance.

12. The semiconductor memory device according to claim 8, wherein each of said memory cells and said reference cell comprises:

a nonvolatile variable resistance element whose electric resistance is changed by an electric stress and remains on the changed electric resistance even after said electric stress is removed; and

a select transistor.

13. The semiconductor memory device according to claim 12, wherein said nonvolatile variable resistance element has a manganese-containing oxide of a perovskite structure formed between electrodes.

14. A method for correcting a reference cell, said reference cell storing a reference level used when reading a data level stored in a plurality of memory cells each capable of storing and programming N-level data, where N is a natural number equal to or greater than 2, the method comprising the steps of:

counting number of times of reading of said reference cell;

determining whether said reference level stored in said reference cell is within a preset range when said number of times of reading that is counted reaches a specified value; and

correcting the reference value to fall within said range if it is determined that said reference level is out of said range.

15. A method for correcting a reference cell, said reference cell storing a reference level used when reading a data level stored in a plurality of memory cells each capable of storing and programming N-level data, where N is a natural number equal to or greater than 2, the method comprising the

steps of:

determining whether said reference level stored in said reference cell is within a preset range, in synchronicity with a synchronous signal output from a timing generation circuit; and

correcting the reference value to fall within said range if it is determined that said reference level is out of said range.